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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/584,601	05/31/2000	Kurt Eisenbeiser	CR00-001	2836

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EXAMINER
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WILSON, SCOTT R

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 08/02/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/584,601

Applicant(s)

EISENBEISER ET AL.

Examiner

Scott R. Wilson

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 01 July 2002.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 14-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10, 12 and 13 is/are rejected.
- 7) ☒ Claim(s) 11 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 May 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other:

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-10, 12 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Kizilyalli et al.. As to claim 1, Kizilyalli et al., Figure 1, discloses a semiconductor device comprising a semiconductor substrate (101), a dielectric layer (102) formed over the semiconductor substrate, which is comprised of a stress-free oxide layer (col. 3, lines 37-58, especially lines 48-51) and a second portion formed with a monocrystalline perovskite material (col. 5, line 39 and col. 7, line 18), where an electric field in the dielectric layer controls the conductivity of the semiconductor substrate. Although not explicitly stated, it is understood in the art that a stress-free oxide layer would necessarily be formed of an amorphous oxide, in contrast with a crystalline material which would have a finite lattice stress.

As to claim 2, the device of Kizilyalli et al. also contains a gate electrode (104), which overlies the dielectric layer and establishes an electric field between itself and the semiconductor substrate.

As to claim 3, the invention referred to in Kizilyalli et al. is a gate structure for a MOSFET (col. 2, lines 11-12), which, although not explicitly stated, is understood in the art to necessarily contain a source, a drain, and a conduction channel therebetween.

As to claim 4, Kizilyalli et al., Figure 1, discloses that the first portion of the dielectric layer (102) is formed adjacent the semiconductor substrate (101), and that the second portion of the dielectric layer (103) is formed between the first portion and the control electrode (104).

As to claim 5, Kizilyalli et al. discloses that the stress-free oxide layer, which is understood in the art to necessarily be amorphous, may be composed of silicon dioxide (col. 3, line 51).

As to claim 6, Kizilyalli et al. discloses the monocrystalline material may be comprised of a perovskite (col. 5, line 39 and col. 7, line 18), some examples of which are known in the art to be lead zirconium titanate (PZT).

As to claim 7, it is understood in the art that the relative permittivity of silicon dioxide, which would be the first portion of the dielectric layer is about 4.0, and the relative permittivity of common perovskites, such as PZT, which would be the second portion of the dielectric layer, is in the hundreds.

As to claim 8, Kizilyalli et al. discloses an example of the thickness of a Ta<sub>2</sub>O<sub>5</sub> dielectric layer being from 30Å to 60Å.

As to claim 9, Kizilyalli et al., Figure 1, discloses a transistor comprising a substrate (101), a gate electrode (104) disposed over the substrate for generating a conduction channel in the substrate in response to a control signal, and a dielectric formed over the conduction channel (102) and (103), the dielectric including a first layer (102) formed with a stress-free layer, which would be understood in the art to be amorphous, and a second layer (103) formed with a monocrystalline perovskite material (col. 5, line 39 and col. 7, line 18) disposed between the first layer and the gate electrode.

As to claim 10, the invention referred to in Kizilyalli et al. is a gate structure for a MOSFET (col. 2, lines 11-12), which, although not explicitly stated, is understood in the art to necessarily contain a source, a drain, and a conduction channel therebetween.

As to claim 12, it is understood in the art that the relative permittivity of silicon dioxide, which would be the first portion of the dielectric layer is about 4.0, and the relative permittivity of common perovskites, such as PZT, which would be the second portion of the dielectric layer, is in the hundreds.

As to claim 13, Kizilyalli et al. discloses an example of the thickness of a  $\text{Ta}_2\text{O}_5$  dielectric layer being from 30Å to 60Å.

#### *Allowable Subject Matter*

Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

*Conclusion*

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 703-308-6557. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-1782.

Application/Control Number: 09/584,601  
Art Unit: 2826

Page 6

srw  
July 31, 2002

NATHAN J. FLYNN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800